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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,358	10/21/2003	Jung Pill Kim	2003P52605US / I331.106.1	4248

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EXAMINER	
NGUYEN, TAN	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 03/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

N/A

Office Action Summary	Application No.	Applicant(s)	
	10/690,358	KIM ET AL.	
	Examiner	Art Unit	
	Tan T. Nguyen	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *8-28* is/are allowed.

6)☒ Claim(s) *1-4 and 6* is/are rejected.

7)☐ Claim(s) *5 and 7* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. The Information Disclosure Statement submitted by Applicants on October 21, 2003 has been received and fully considered.

2. The disclosure is objected to because of the following informalities:

In page 6, line 13; line 27; page 7, line 12; page 9, line 10; line 20; page 10, line 1, the number "44" for the OE signal should be changed to --43--. In page 6, line 13; line 27; page 7, line 12; page 9, line 10; line 20; page 10, the number "46" for the DATA SIGNAL should be changed to --44--. In page 6, line 20; page 7, line 3; line 7, the number "38" for VDDQ should be changed to --46--.

Appropriate correction is required.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Lewis et al. (U.S. Patent No. 5,995,440).

Lewis et al. disclosed in Fig.1 a memory device having a voltage sensing circuit [10] for detecting the external voltage VCC applied to the memory chip et input terminal [8] and generates an output adjust signal [VADJ] (column 2, lines 45-48). Lewis et al. further disclosed in Fig.2 an off-chip driver circuit (OCD) [44] coupled to the output adjust signal [VADJ] from the voltage sensing circuit [10]. The output adjust signal [VADJ] is used to adjust the performance of the OCD circuit [44] (column 3, lines 36-40). As shown in Fig.2, the OCD circuit [44] generates an output at the terminal [DQ].

Although Lewis et al. did not disclose the output signal DQ is adjusted by adjusting the magnitude of at least one impedance, Lewis disclosed based on the state of the output adjust signal [VADJ], the transistors [58, 60, 62] are turned ON or OFF, which inherently adjusts the impedance of the OCD circuit [44] (column 3, lines 44-66). Furthermore, although Lewis et al. did not show a memory array but any DRAM circuit inherently includes a memory array.

Regarding claim 2, Lewis et al. disclosed the OCD circuit is used in a DRAM circuit (column 1, lines 7-10).

Regarding claim 3, Lewis et al. showed in Fig. 2a and @b, the OCD circuit [44] includes a plurality of transistors.

Regarding claim 4, the output signal at the terminal [DQ] would be current or voltage.

Regarding claim 6, Lewis et al. disclosed the slew-rate of the output signal at terminal [DQ] is changed in response to the output adjust signal [VADJ].

5. Claims 4 and 7 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 8-28 are allowed.

7. The following is an examiner's statement of reasons for allowance:

The prior art did not show or suggest the OCD couples the output node to the source voltage or the reference node via the first or second impedance, respectively, according to the state of the data signal.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

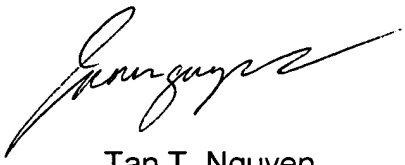
8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Yoo et al. is cited to show a memory device having a power supply voltage level detector. Suzuki is cited to show a semiconductor device having an impedance adjustment control circuit.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tan T. Nguyen whose telephone number is (571) 272-1789. The examiner can normally be reached on Monday to Friday from 07:00 AM to 03:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho, can be reached at (571) 272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tan T. Nguyen
Primary Examiner
Art Unit 2827
March 04, 2005